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	instruction 1	instruction 2	
0	add	<i>nop</i>	← P0
2	<i>nop</i>	mpy	← P1
4	<i>nop</i>	load	← P2

Fig.1(A)

before compaction

0	add
1	<i>nop</i>
2	<i>nop</i>
3	mpy
4	<i>nop</i>
5	load

Fig.1(B)

after compaction

0	100101	key
1	add	
2	mpy	
3	load	

Fig.1(C)

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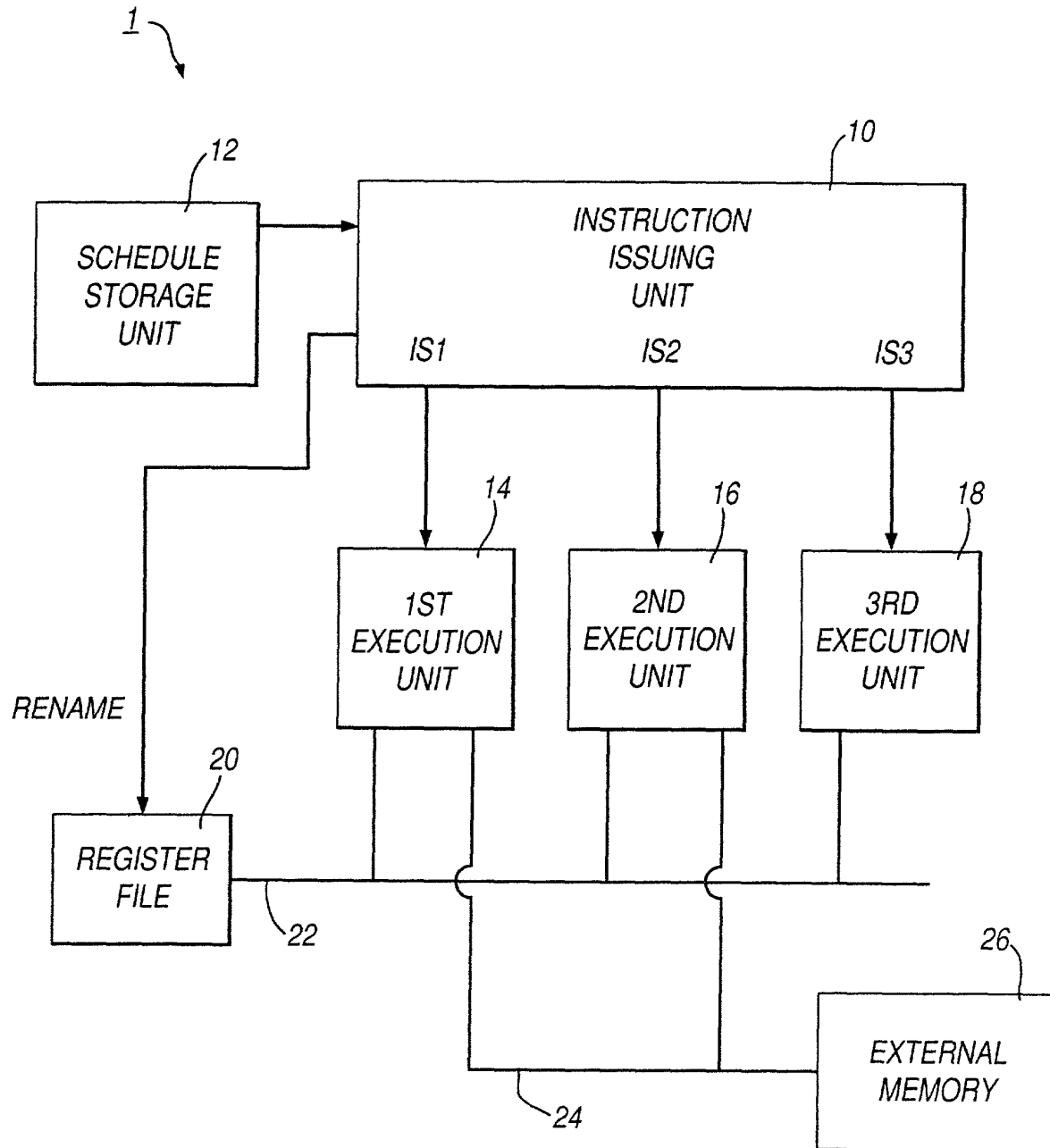


Fig.2

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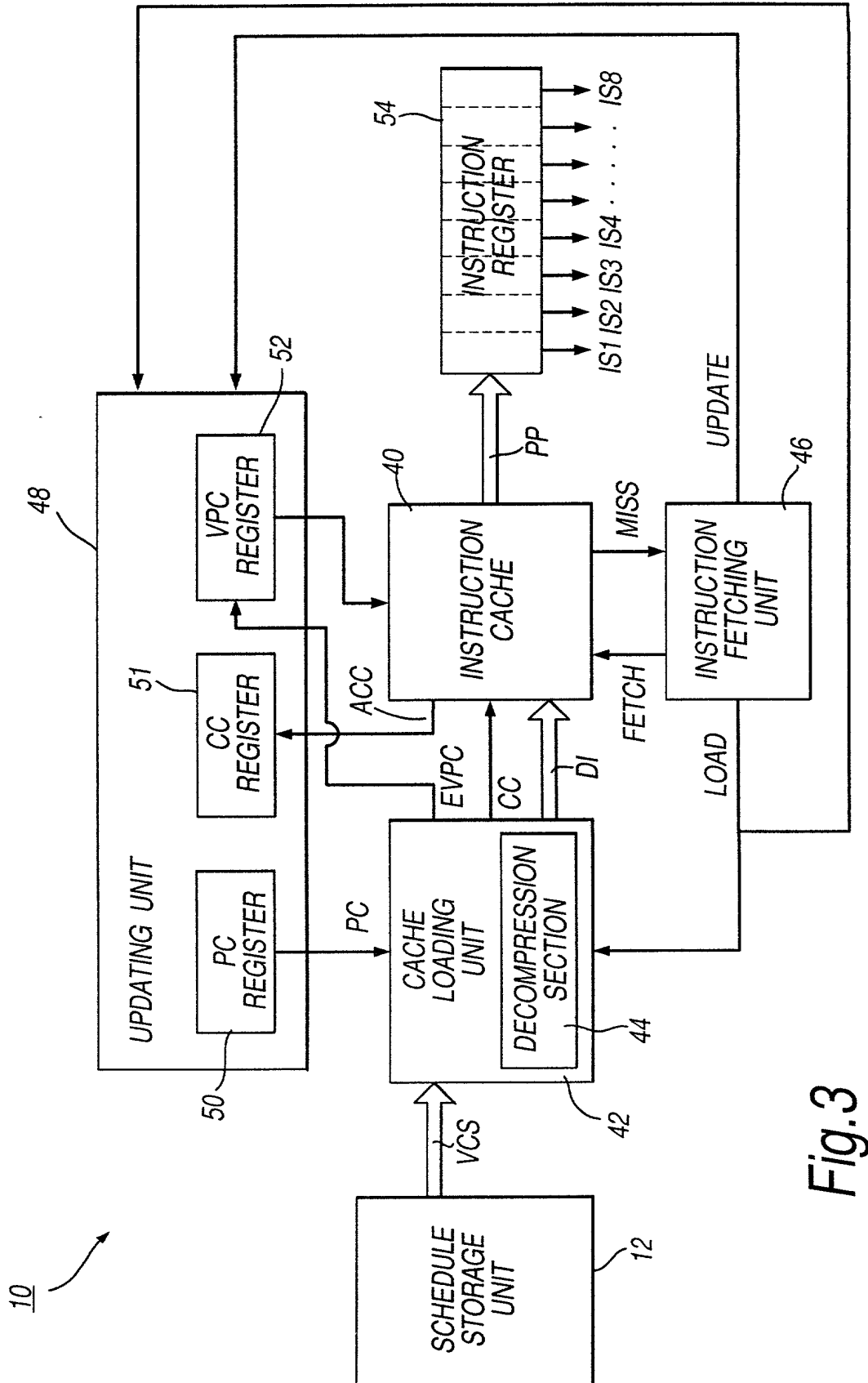


Fig.3

FIG. 3 is a block diagram of a processor architecture.

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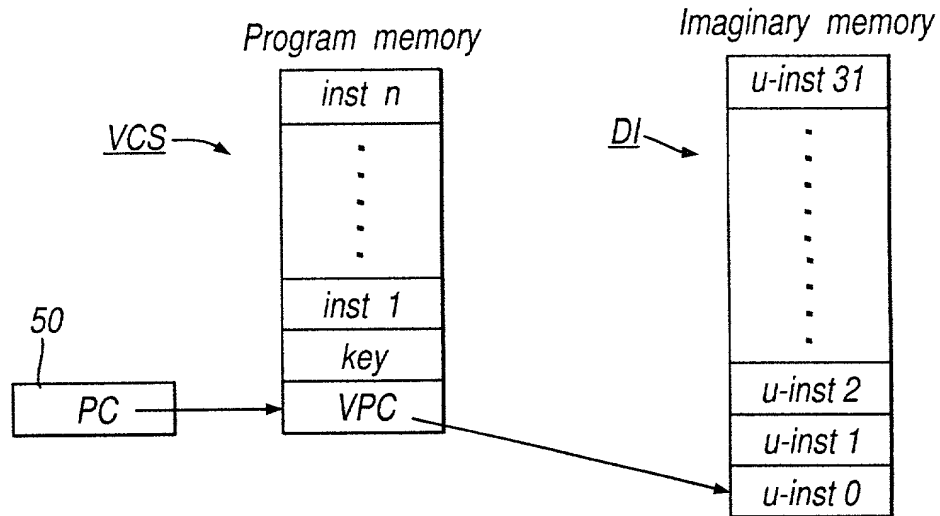


Fig.4

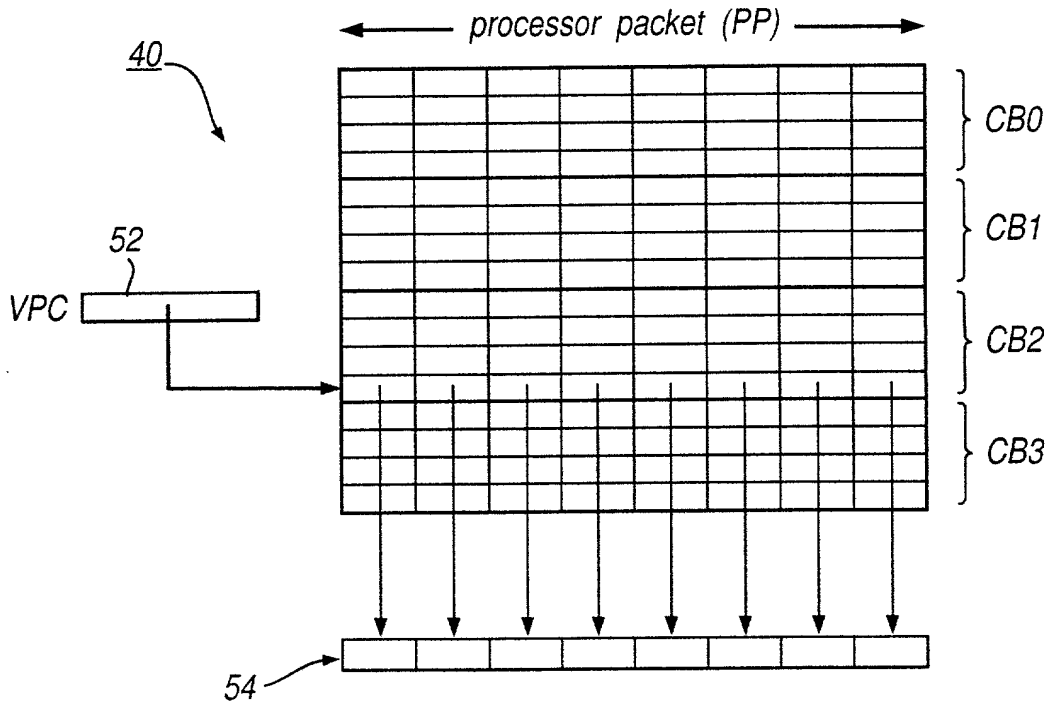


Fig.5

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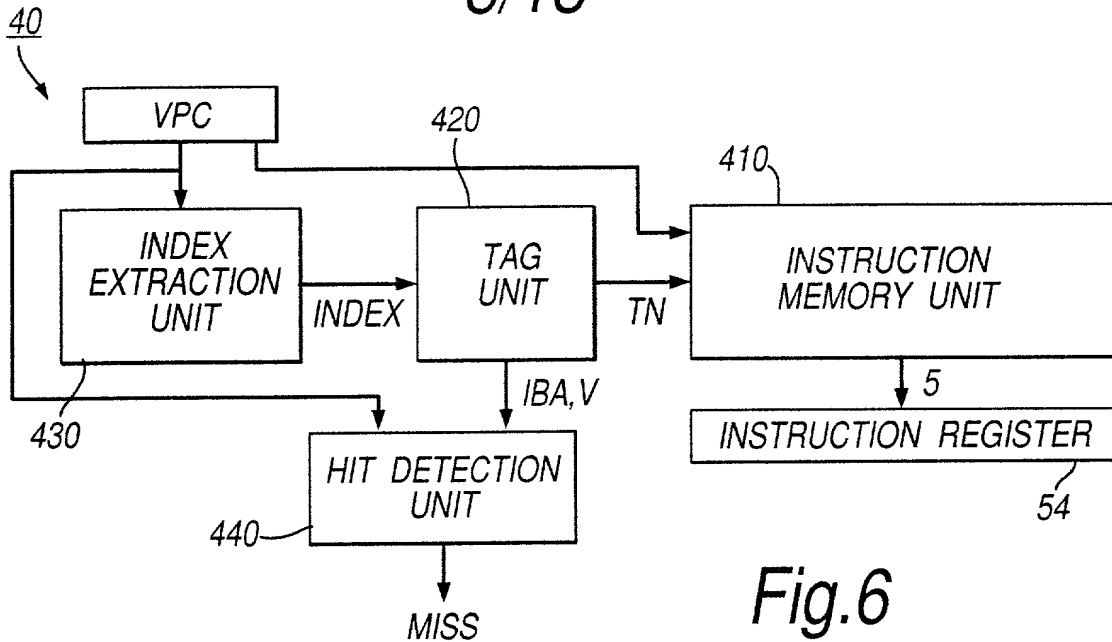


Fig.6

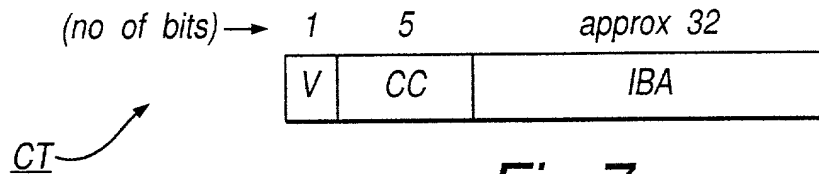


Fig.7

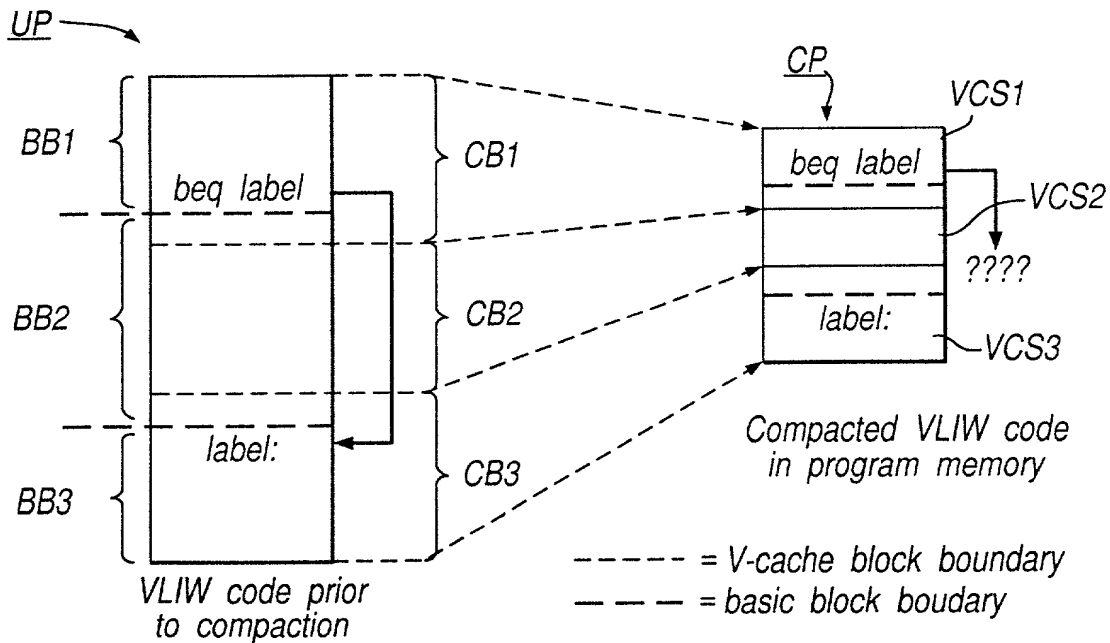


Fig.9

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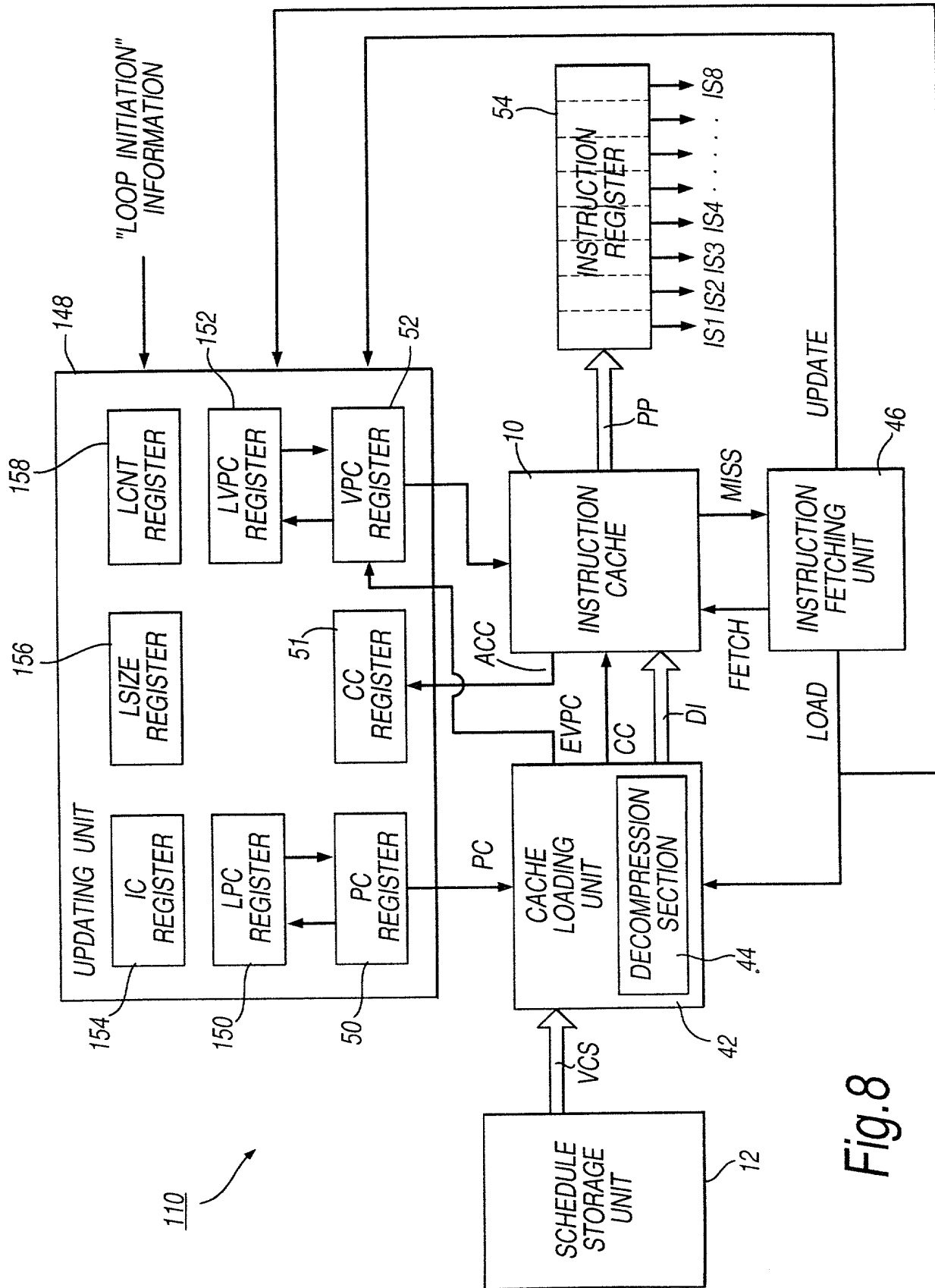


Fig.8

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loop:	-	l1	l2	-	1000
	loop 8, r1	-	-	-	1010
	l3	l4	-	-	1020
	-	l5	-	l6	1030
	-	l7	-	-	1040
	l8	l9	-	-	1050
	-	l10	-	l11	1060
	-	-	-	l12	1070
	-	l13	l14	-	1080
	l15	-	l16	-	1090
	-	l17	-	l18	10a0
	l19	-	-	l20	10b0

Fig.10

VCS1	1000	2000
	key1	2004
	l1	2008
	l2	200c
	loop 8, r1	2010
	l3	2014
	l4	2018
	l5	201c
VCS2	l6	2020
	1040	2024
	key2	2028
	l7	202c
	l8	2030
	l9	2034
	l10	2038
	l11	203c
VCS3	l12	2040
	1080	2044
	key3	2048
	l13	204c
	l14	2050
	l15	2054
	l16	2058
	l17	205c
	l18	2060
	l19	2064
	l20	2068

Fig.11

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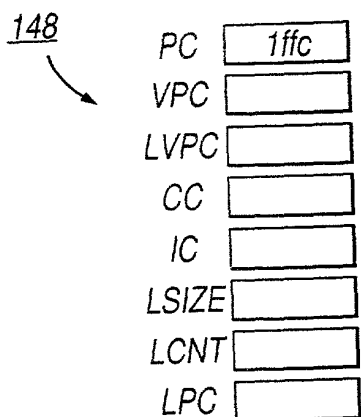
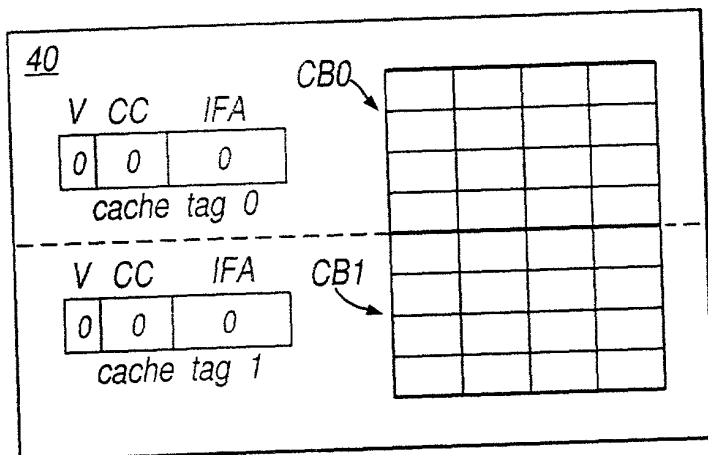


Fig.12

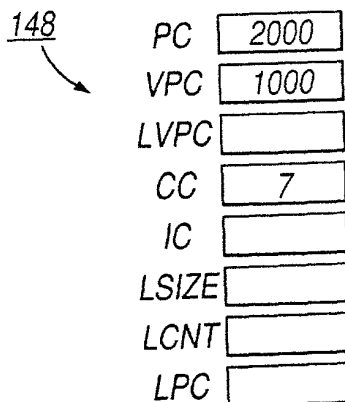
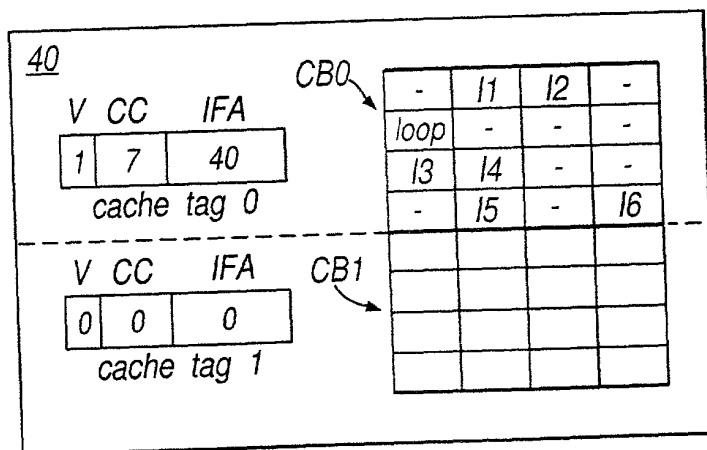
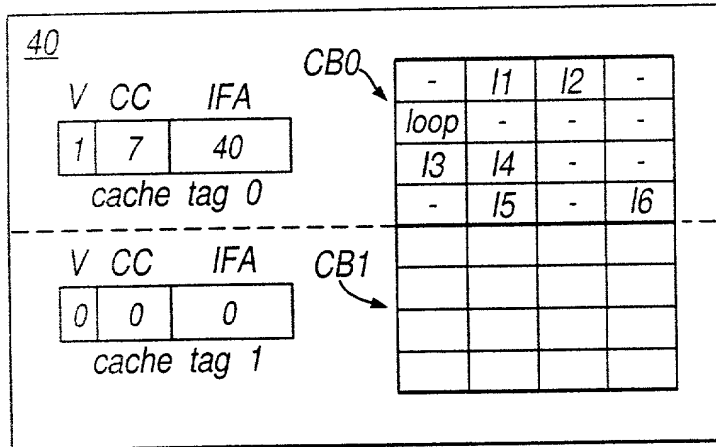


Fig.13

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PC 2000

VPC 1020

LVPC 1020

CC 7

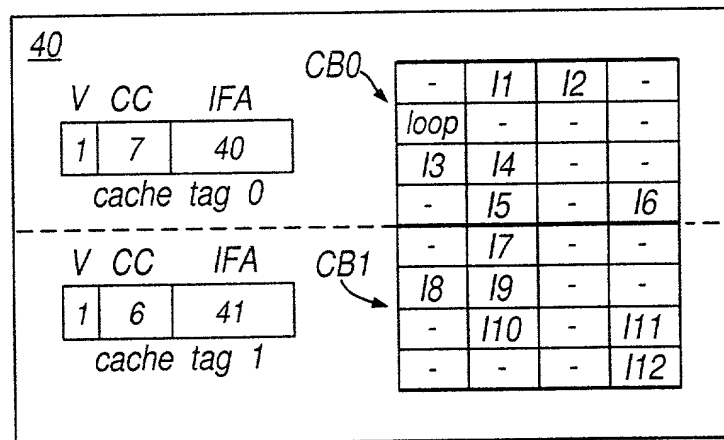
IC 42

LSIZE 8

LCNT 8

LPC 2000

Fig. 14



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PC 2024

VPC 1040

LVPC 1020

CC 7

IC 42

LSIZE 8

LCNT 6

LPC 2000

Fig. 15

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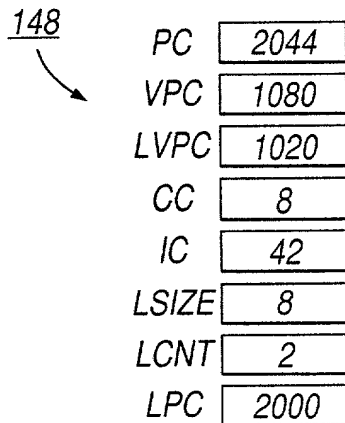
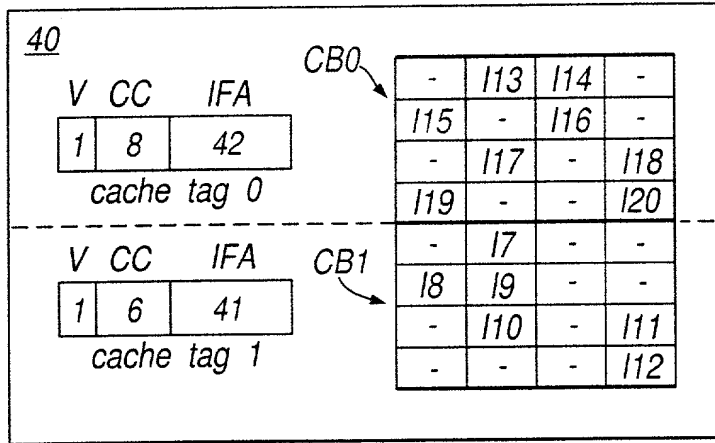


Fig. 16

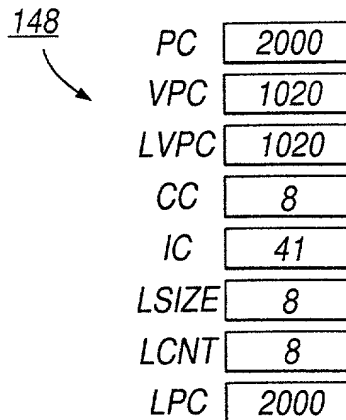
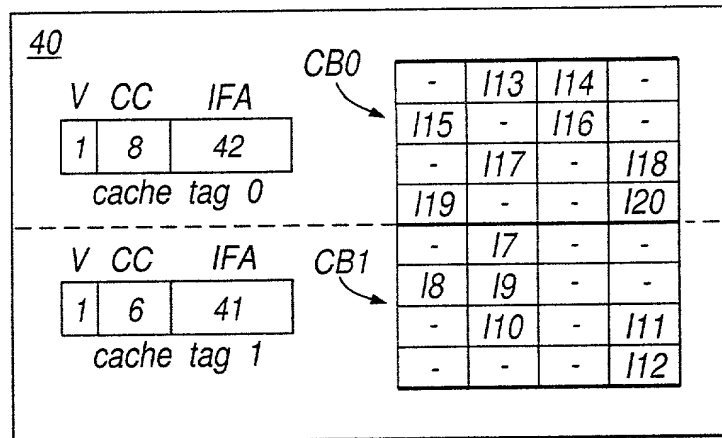


Fig. 17

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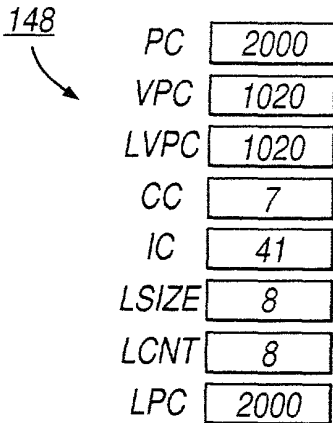
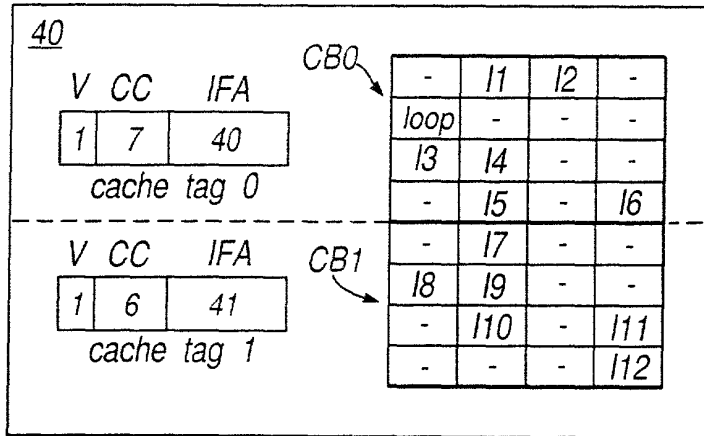


Fig.18

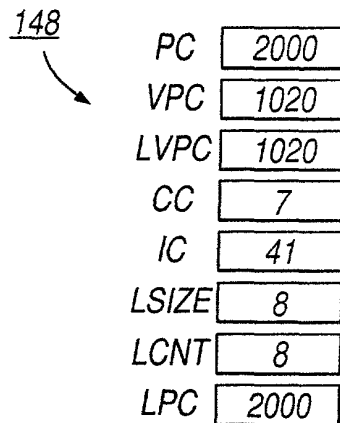
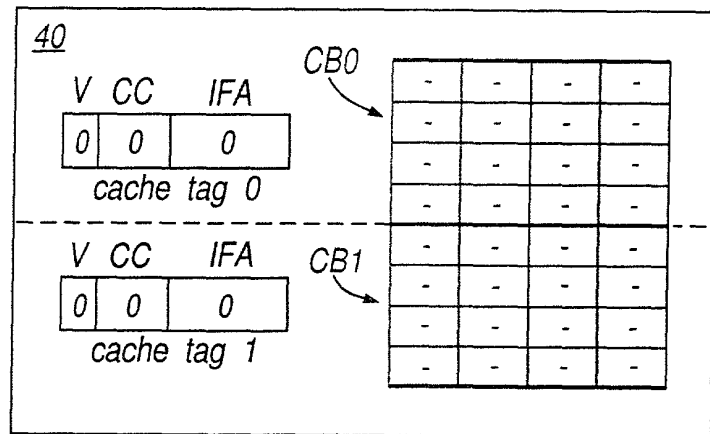


Fig.19

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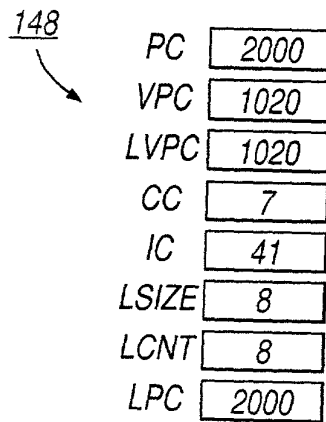
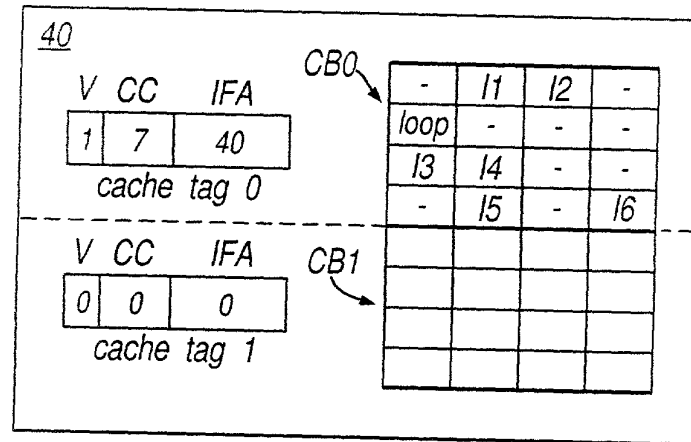


Fig.20

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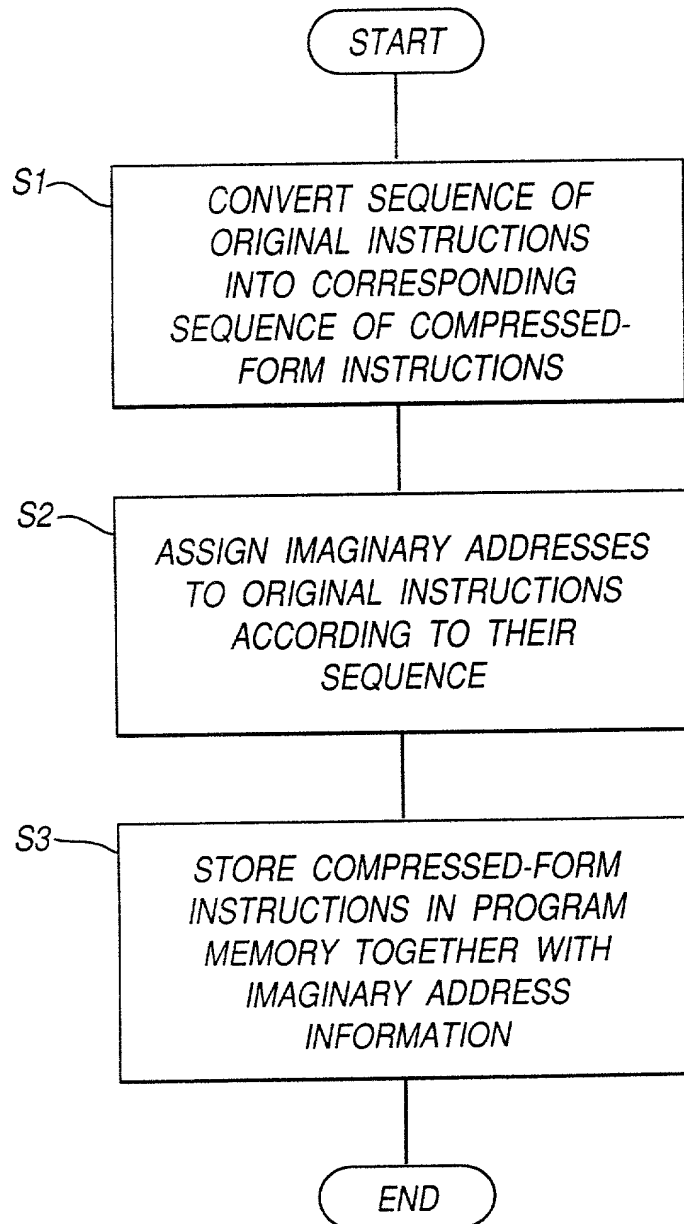


Fig.21